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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN THE APPLICATION OF:

BIN-SHING CHEN

SERIAL NO.: 09/769,576

FILED: January 25, 2001

FOR: METHOD FOR MANUFACTURING
SPLIT-GATE EEPROM MEMORY
CELL AND STRUCTURE FORMED
THEREBY

Group Art Unit 2811

Examiner Thien F. Tran

#610
8/28/2
RECEIVED
TECHNOLOGY CENTER 2800
AUG 22 2002

AMENDMENT

Box Non-Fee
Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

In The Title

Please amend the title to "STRUCTURE OF SPLIT-GATE EEPROM MEMORY
CELL".

In The Abstract

Please amend the abstract to "the present invention concerns the structure of a self-aligned split-gate EEPROM memory cell. The memory cell has a cell size smaller than the traditional split-gate structure without sacrificing program disturb immunity and includes a silicon substrate having a source/drain region, a tunnel oxide layer disposed over the silicone substrate, a select gate disposed over the tunnel oxide layer. The select gate is defined by a conductive layer covered with a first insulated material and includes a sidewall